Raymond Tang

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IC Mask Designer

Versatile IC Mask Designer with expertise in custom high speed mixed signal analog, custom digital control and datapaths, and digital automated place and route. Proficient in all levels of hierarchy from full chip integration and package considerations down to standard cells, and top down and bottom-up floor planning. Expertise in design techniques, parasitic effects, and validation. Driven to produce quality designs while meeting deadlines and expectations. Experienced in various CMOS process nodes from 180nm to 28nm, trained in FinFET processes with 7nm to 3nm considerations, creative in debugging and problem solving, and eager to learn and adapt to new methodologies and technologies.

AREAS OF EXPERTISE

IC Custom Analog/Digital Layout Design · IC Physical Design · Project Management
Linux Administration · Network Infrastructure · Remote Virtual Machines · System Administration

TECHNICAL SKILLS

Software

Cadence Virtuoso XL · Mentor Calibre Physical Verification
Cadence RTL-to-GDS · Synopsys RTL-to-GDS · Synopsys Hercules Physical Verification · SFT R3D / RMAP

Development

Skill / Lisp · TCL · Verilog · RTL · Java · Python · Perl · Javascript · HTML · CSS · SQL
git · SVN · Perforce · Cliosoft SOS · Confluence

PROFESSIONAL EXPERIENCE

IC Mask Designer / Owner

Poligon Designs, Salt Lake City, UT *January 2024 – Present*

Providing IC mask design services while adapting to different technologies, methodologies, and procedures

- Analog Layout Designer: Contractor – *Polygon IC*
  Cirrus Logic *January 2024 – August 2024*

  Provide block level analog layout design, full chip integration collaboration, and test structure development. Verify designs with Calibre LVS and DRC, and Silicon Frontline Technology R3D, and RMAP.

  - Designed in Tower 55nm process
  - Learned, assisted in debugging, and guided others in the use of R3D
  - Developed scripts to increase task completion efficiency

IC Mask Designer

Analog Devices, Inc. *April 2001 – November 2023*

As project lead, coordinated the efforts of the layout team, as well as supported the needs of the Digital APR, DV, and PTE teams while floorplanning analog layout, building sub blocks, and maintaining full chip interconnect. Validated designs with Calibre LVS and DRC in multiple sub micron process nodes. Expertise in design techniques such as common centroid matching and interdigitation, while cognizant of EMIR, DFM, ERC, PERC, and ESD considerations

and efficiently utilizing and minimizing area usage. Experienced in digital implementation and timing closure. Created documentation for design reviews and procedures.

- Designed in TSMC 180nm automotive, TSMC 130nm through 28nm, and GF 55nm processes
- Closely collaborated with designers for efficient turnaround and high-quality designs
- Contributed code to the site's Cadence Virtuoso environment to boost productivity
- Merged custom and automation elements allowing greater layout design flexibility
- Contributed to digital implementation flow development
- Collaborated in digital-on-top chip design
- Maintained a 100% track record of meeting deadlines
- Provided onsite IT support including hardware and software installation, network configuration, and Linux administration

ADDITIONAL RELEVANT EXPERIENCE

Field Technician
teXolutions, Inc.

Performed DSL installation including running cable from the DMARC, hardware configuration, and system testing. Troubleshot connectivity issues with the internet provider at customer site and telecommunication center.

- 99% success rate of installations and service calls

Technical Support
Packard Bell NEC / Alorica

Provided technical support to customers and mentor support to technical support representatives. Experienced in customer service and sales.

EDUCATION

Bachelor of Science (BS) in Computer Science
Minor in Mathematics, *Cum Laude*
Westminster College, Salt Lake City, UT

Associate of Applied Sciences (AAS) in Electronic Technology
Honors
ITT Technical Institute, Murray, UT

CERTIFICATIONS

FinFET Layout	**IC Mask Design**
A+	**CompTIA**

VOLUNTEER EXPERIENCE

Field of Dreams	**Habitat for Humanity**, Salt Lake City, UT
Jordan River Walk	**Jordan River Commission**, West Jordan, UT

INTERESTS

Home Lab · Electronics · Photography · Woodworking · Cooking · Golf · Snowboarding · Travel